

REMARKS

The Office Action dated December 13, 2005, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-10 and 16-23 have been allowed Claims 11-15 are submitted for consideration.

Claims 13 and 15 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Based on the arguments presented below, Applicant requests that this objection be withdrawn.

Claims 11, 12 and 14 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,754,216 (Wong). The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in independent claims 11, 12 and 14.

Claim 11, upon which claims 12-15 depend, recites a method for communication of rate control messages between two switches. The method includes the steps of designating a first plurality of ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme. The method also includes coupling a first link port of the first plurality of ports to a second link port of the second plurality of ports and configuring the first switch to generate a first rate control message at the first switch and relay the first rate control message to a first local communications channel of the first port. The method further includes configuring the first switch to perform a rate control function related to the second switch based on the first rate control message.

As outlined below, Applicant submits that the cited reference of Wong does not teach or suggest the elements of claim 11.

Wong teaches a switch fabric in communication with an Ethernet switch system. The switch fabric includes a switch processor, a memory and a FAD transceiver system for receiving and transmitting streams of cells over a high-speed data bus. The FAD transceiver includes a plurality of receive and transmit buffers, where there exists a set of buffers for every multiplex device with which the FAD is to communication. The FAD includes a logic unit, a receive buffer, a unicast transmit buffer and a multicast transmit buffer. The Ethernet switch system includes a plurality of multiplex devices that receive and transmit data packets from the FAD system and that are coupled to a plurality of Ethernet switches that route packets to external devices connected thereto. Col. 7, line 66-Col. 8 line 36 and Figure 3.

Wong further teaches that the switch processor communicates with the memory to obtain memory status information and to the logic unit of FAD. The switch processor controls signals to the logic unit for controlling the transmission and reception of packets and for storage and retrieval from the memory. Col. 8, lines 48-60. Figure 4 shows the switch fabric in communication with a plurality of external devices for receiving and transmitting data. As shown in figure 4, FAD include three groups of buffers, the first group being receive buffers, the second group being unicast transmit buffers and the third group being multicast transmit buffers. Col. 9, line 53-Col. 10, line 5.

Applicants submit that Wong simply does not teach or suggest each of the elements recited in claim 11. Claim 11, in part, recites designating a first plurality of ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme. The Office Action alleges that the first plurality of ports of the present invention is equivalent to the FAD buffers of Wong. As is known to those skilled in the art, a port of a switch is an interface on a switch to which other devices can be connected. A buffer, on the other hand, is known to those skilled in the art as a temporary storage area. Thus, one skilled in the art would not equate the buffers of Wong with the first plurality of port of the present invention because they are different components that perform different functions. Col. 12, lines 28- of Wong disclose that the multiplex devices of figure 4 are connected to the buffers of the FAD, on one end, and, on the other end, to port interface device chips (OctaPIDs), each of which include eight port interface device that are coupled to communicate with a plurality of different Ethernet switches. Therefore, Applicant submits that even the teachings of Wong show the difference in the functions of a port and a buffer. Applicant submits that, if as the Office Action alleges the switching fabric of Wong is equivalent to the first plurality of ports of the present invention, then there is simply no teaching or suggestion in Wong of designating a first plurality of ports of a first switch by a first numbering scheme, and designating a second plurality of ports of a second switch by a second numbering scheme, as recited in claim 11.

Furthermore, claim 11, in part, recites configuring the first switch to generate a first rate control message at the first switch and relay the first rate control message to a first local communications channel of the first port. The Office Action alleges that the local communications channel of the present invention is equivalent to the switch process of Wong. As is known to those skilled in the art, a local communications channel of a switch is a transportation path for sending a message. A processor, on the other hand, is known to those skilled in the art as a unit that controls logic. Thus, one skilled in the art would not equate a local communications channel recited in claim 11 with a processor disclosed in Wong because they are different components that perform different functions. Col. 8, lines 48-58 of Wong disclose that the switch processor is **not** in the data path of the switch fabric; rather, the switch processor communicates with the memory to obtain information and communicates with the logic unit to control the transmission and reception of data packets. Therefore, Applicant submits that even the teachings of Wong shows the difference in the functions of a local communication channel of the present invention and the switch processor disclosed in Wong. Applicant submits that Wong simply does not teach or suggest configuring the first switch to generate a first rate control message at the first switch and relay the first rate control message to a first local communications channel of the first port, as recited in claim 11 and alleged by the Office Action. Therefore, Applicants respectfully assert that the rejection under 35 U.S.C. §102(e) should be withdrawn because Wong fails to teach or suggest each feature of claim 11, and the dependent claims thereon.

As noted previously, claims 11-15 recite subject matter which is neither disclosed nor suggested in the prior art references cited in the Office Action. It is therefore respectfully requested that all of claims 11-15, in addition to claims 1-10 and 16-23, be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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